

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Hideki MASUDA et al.)
) Group Art Unit:
Application No.: Not Yet Assigned)
) Examiner:
Filed: January 15, 2004)
)
For: METHOD OF)
MANUFACTURING)
SEMICONDUCTOR DEVICE)
AND SEMICONDUCTOR
DEVICE

MAIL STOP PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. A copy of the document listed under Other Documents is attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

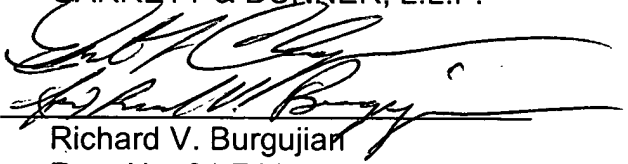
If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: January 15, 2004

By:


Richard V. Burgujian
Reg. No. 31,744

Enclosures
RVB/FPD/gah

ERNEST F. CHAPMAN
Reg. No. 25,961

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	05225.0257	Application No.	
Applicant	Hideaki MASUDA et al.		
Filing Date	January 15, 2004	Group:	

U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
	6,287,973 B2	09/11/2001	Aoi			

FOREIGN PATENT DOCUMENTS						
Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Hasegawa et al.; "COPPER DUAL DAMASCENE INTERCONNECTS WITH LOW-K ($K_{EFF} < 3.0$) DIELECTRICS USING FLARE™ AND AN ORGANO-SILICATE HARD MASK"; International Electron Devices Meeting (IEDM), pages 623-626, (1999)

Examiner	Date Considered
<p>*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce